IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Douglas J McKenney et al.	:	Date: 30 November 2006
Group Art Unit:	2825	:	LSI Logic Corporation
Examiner:	Stacy Whitmore	:	Intellectual Property Law
Serial No.:	10/713,492	:	1621 Barber Lane
Filed:	14 November 2003	:	MS D-106
Confirmation No.	9210	:	Milpitas, CA 95035

Title: FLEXIBLE DESIGN FOR MEMORY USE IN INTEGRATED CIRCUITS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

DECLARATION UNDER 37 CFR §1.131

We, Douglas J McKenney and Steven M. Emerson, state as follows:

1. We are the inventors of claims 1-20 in the above identified patent application and the inventors of the subject matter described and claimed therein.

2. Prior to 09 December 2002 and during all relevant times during the invention of the subject matter described and claimed in the above-identified patent application, we were employed by LSI Logic Corporation (LSI), the assignee herein, at LSI's Processor Cores Technology Group development facility in Bloomington, Minnesota. The activities relating to the invention of the subject matter of this patent application occurred at the aforementioned LSI facility.

3. Prior to 09 December 2002, we invented the invention described and claimed in the above-identified patent application.

4. Pursuant to our obligation to disclose inventions that are made in the course of our employment with LSI, we disclosed the subject matter of our invention to LSI's Intellectual Property Law department on or before 09 December 2002. As evidence of invention, we submit Exhibit A, pages 1-18 of an invention disclosure entitled *A Method for Flexible Memory Use in RapidChip™ Devices*, which is dated prior to 09 December 2002. These pages disclose a method of designing an integrated circuit having a flexible memory used for a range of processing functions and memory requirements. All the redacted dates are prior to 09 December 2002 and Exhibit A is a true and correct copy of the relevant portions of the document.

5. LSI's Intellectual Property Law began review of the disclosure and preparation of a patent application on the subject matter of the invention. The patent application was filed on 14 November 2003.

6. We acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both under 18 U.S.C. 1001. We acknowledge that willful false statements may jeopardize the validity of the application or any patent issuing thereon.

7. All statements of this declaration made of our own knowledge are true and all statements made on information and belief are believed to be true.

Declaration under 37 CFR 1.131
Inventor 1 of 2

SIGNATURE:
Inventor (1) Signed at Bloomington, Minnesota

on 11/30/2006

Douglas J McKenney

Douglas J McKenney

Declaration under 37 CFR 1.131
Inventor 2 of 2

SIGNATURE:
Inventor (2) Signed at Bloomington, Minnesota

on 12/1/06

Steven M. Emerson

Exhibit A
Serial No. 10/713,492
Docket No. LSI 03-0085

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Patent Disclosure

LSI LOGIC ®

A Method for Flexible Memory Use in RapidChip™ Devices

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2.0. Dates:

Conception:

Reduction to practice:

trial layout only,

Disclosure of Invention:

none outside of LSI

Sale or offer for sale of invention:

none

Use of invention:

This invention has not been used yet.

3.0. Prior Art

No knowledge

4.0. Background of Invention

Complex functions that include multiple memory blocks are embedded in cell based logic or base transistors (custom logic). This logic is fixed and cannot be changed without a complete respin of the silicon device. This complex function may not be wanted by all users of the silicon device. In this case the logic cannot be reused.

Current practice in the industry today is to either fix the function in base transistors, or implement the function in programmable logic (fpga). The first approach is inflexible. If the customer decides they don't want to use the function, the area is wasted. The second approach is highly flexible, but is less area efficient and achieves much lower performance (speed).

This invention addresses the issues with both approaches. If the customer decides not to use the function, the memories and logic can be reused for some other application. The solution is more area efficient and higher performance than FPGA logic.

5.0. Details of Invention

This invention enables reuse of memory blocks for multiple functions, therefore making the most efficient use of the silicon resources.

5.1 Features of Invention

A set of similar functions may use a very similar set of memory blocks. This invention outlines a methodology for creating multiple functions that can be mapped onto this set of memory blocks. The memory block set is defined as the largest common denominator across all functions to be mapped. This set of memory blocks is then placed and routed using the largest common denominator of logic. This defines the fixed placement of the memory blocks, since they are embedded in the base layers of the silicon device.

In the case of a single memory block, multiple functions can also be mapped to this block.

The logic devices used in this invention are logic array (RapidChip) elements. These are metal programmable logic elements. The use of the memory blocks is defined by the metal programming of these logic elements. Multiple functions can then be mapped to the memory blocks.

5.2 Examples

All memories considered here are single port synchronous memories. The memories have one address bus, write data input bus, read data output bus, and a write enable pin(s). The memories are synchronous, so they have a clock. The invention can be extended to cover any type of memory array (dual port, multi port) in which the use of the memory is defined by the metal programming of the logic array.

5.2.1 Microprocessor

A microprocessor may contain cache memory blocks. Several microprocessors may use similar sized memories for the tag and data set memories of a cache subsystem. This invention outlines a way to choose the largest common denominator of memory blocks so that one of many types of microprocessors can be implemented in the available logic array.

In the case of ARM microprocessors, ARM966, ARM946, ARM926 and ARM1026 processors can all be mapped to the same set of memories.

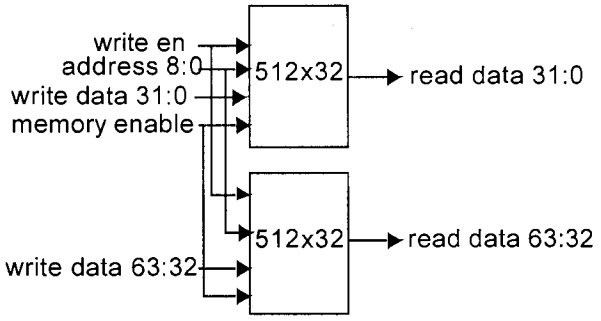
Table5.1 Microprocessor with 16KB caches example

ARM Processor	Inst Tag size (4)	Inst Set size (4)	Data Tag size (4)	Data Set size (4)	Valid size (2)	Dirty size (1)	MMU
ARM1026EJ-S	128x22	512x64	256x22	512x64	32x24	128x8	32x128
ARM926EJ-S	128x22	1024x32	128x22	1024x32	32x24	128x8	32x112
ARM946ES	128x20	1024x32	128x20	(8)512x32	-	128x8	
ARM966ES (no cache)	Uses any size 32 bit wide memory on either data or instruction side. In this case, 16KB is available for instruction or data TCM						
Memory superset	(4)128x22	(8) 512x32	(4)256x22	(8)512x32	(2)32x24	128x8	(4)32x32

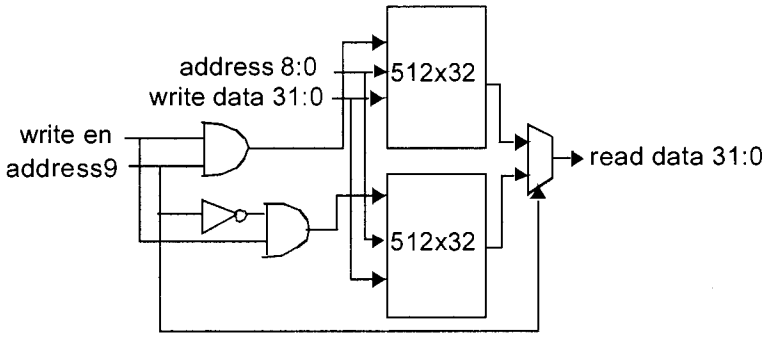
The following figures demonstrate how a set of memories with fixed placement can be used to implement all of these ARM processors. The memory superset includes memory sizes and configurations that can be configured with logic and interconnect to create the memories needed for each microprocessor.

Figure5.1 Instruction or Data Set Memory Configuration Example

ARM1026EJ-S 512x64 Instruction or data set memory created from 2 512x32 memories fixed in the base layers.



ARM946ES Instruction memory or ARM926EJ-S 1024x32 Instruction and data set memory created from 2 512x32 memories fixed in the base layers.



ARM946ES 512x32 data set memory uses the 512x32 memories fixed in the base layers as is.

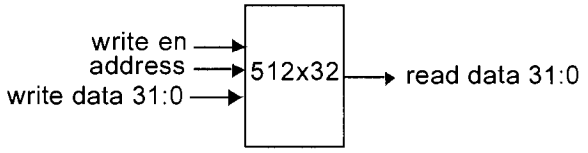


Figure5.2 ARM1026EJ-S Microprocessor with 16KB caches

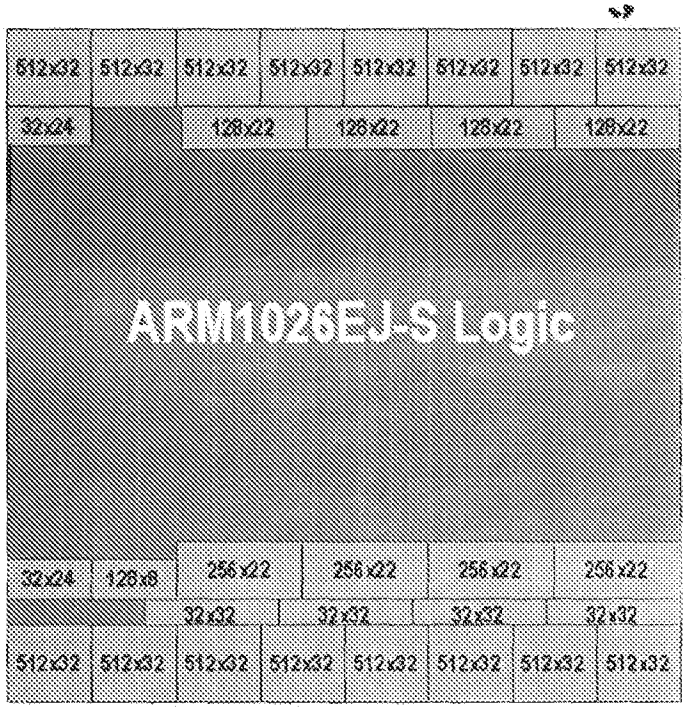


Figure5.3 ARM926 EJ-S Microprocessor with 16KB caches

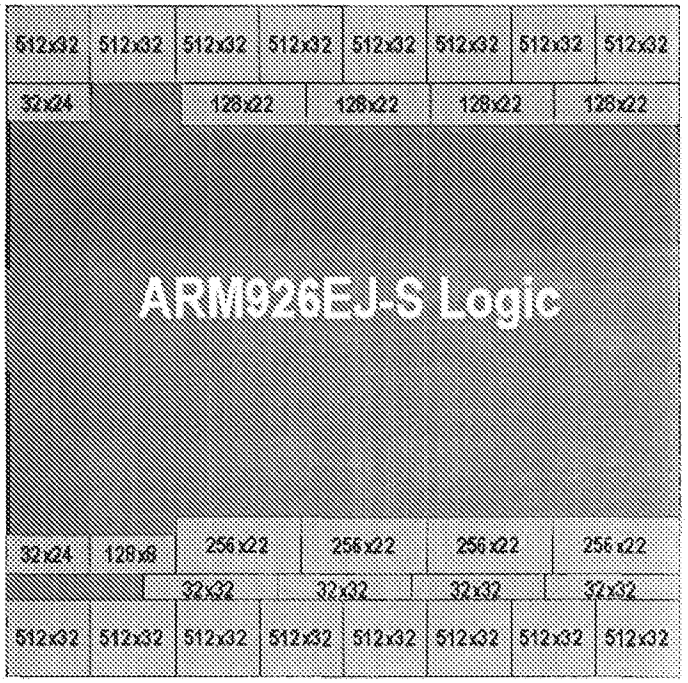


Figure5.4 ARM946ES Microprocessor with 16KB caches (unused memory in red)

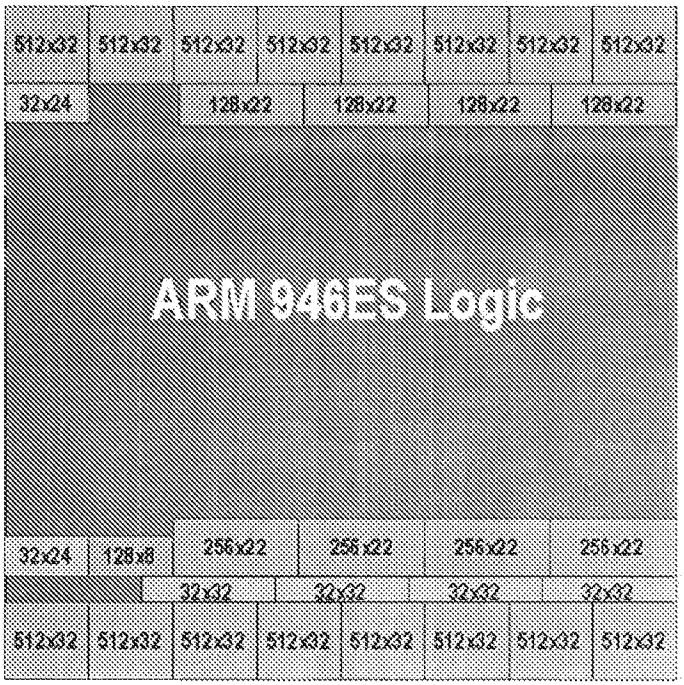


Figure5.5 ARM966ES Tightly Coupled Memory Configuration Example

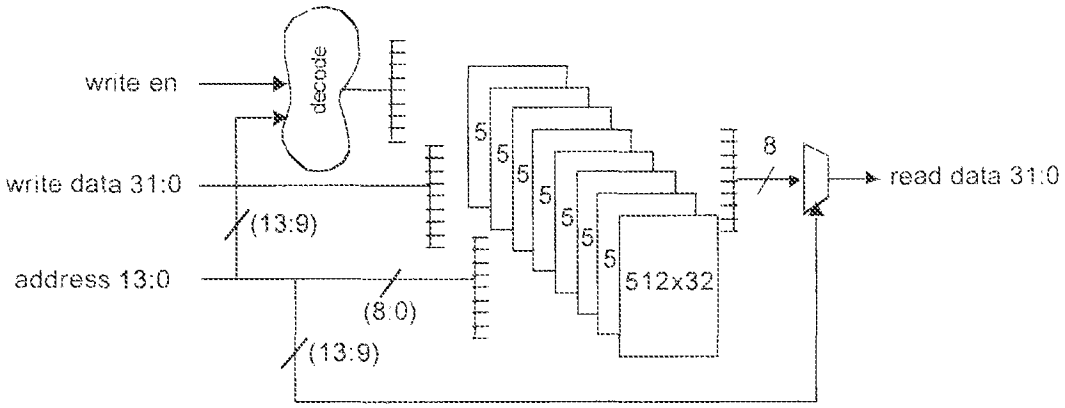


Figure5.6 ARM966ES Microprocessor with 16KB TCMs (unused memory in red)

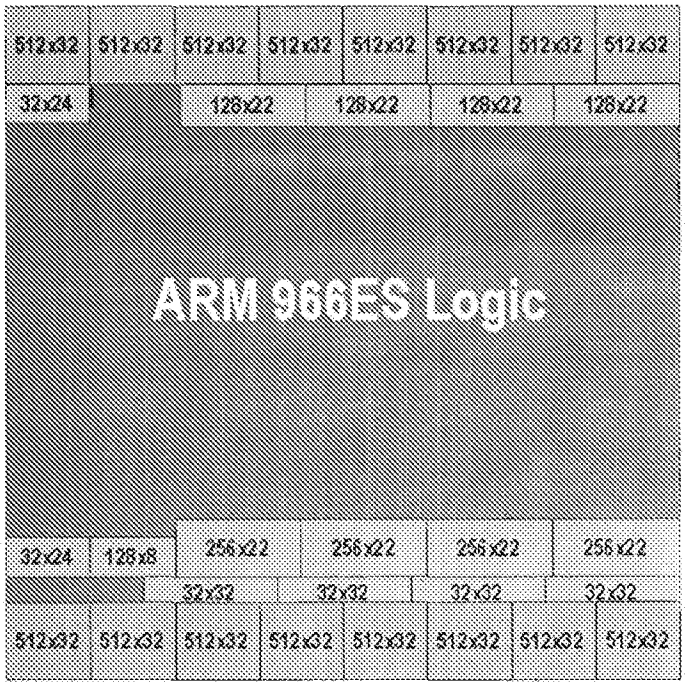


Figure5.7 Memories are unused, and logic array is used for another application (unused memories in red)

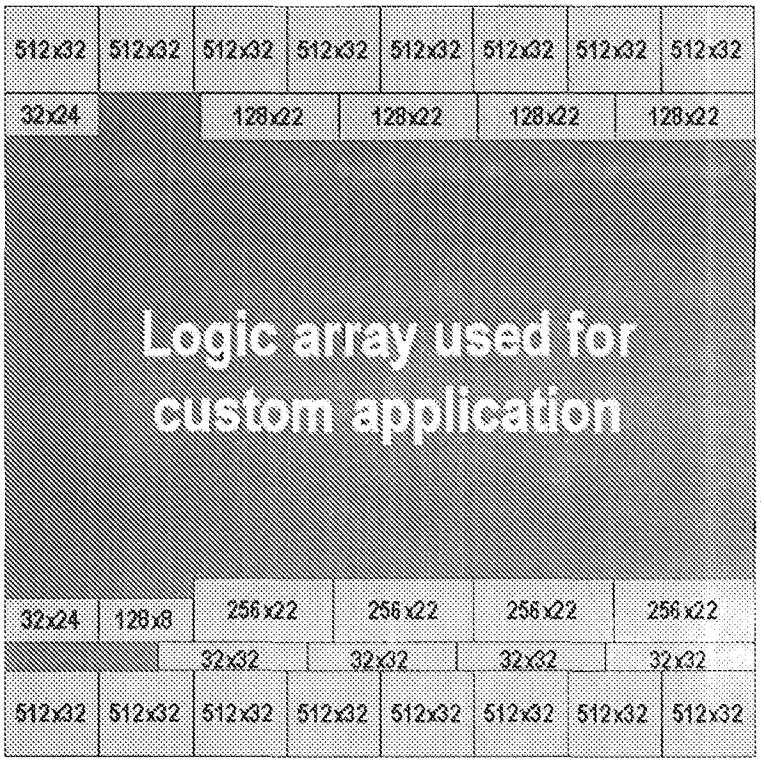
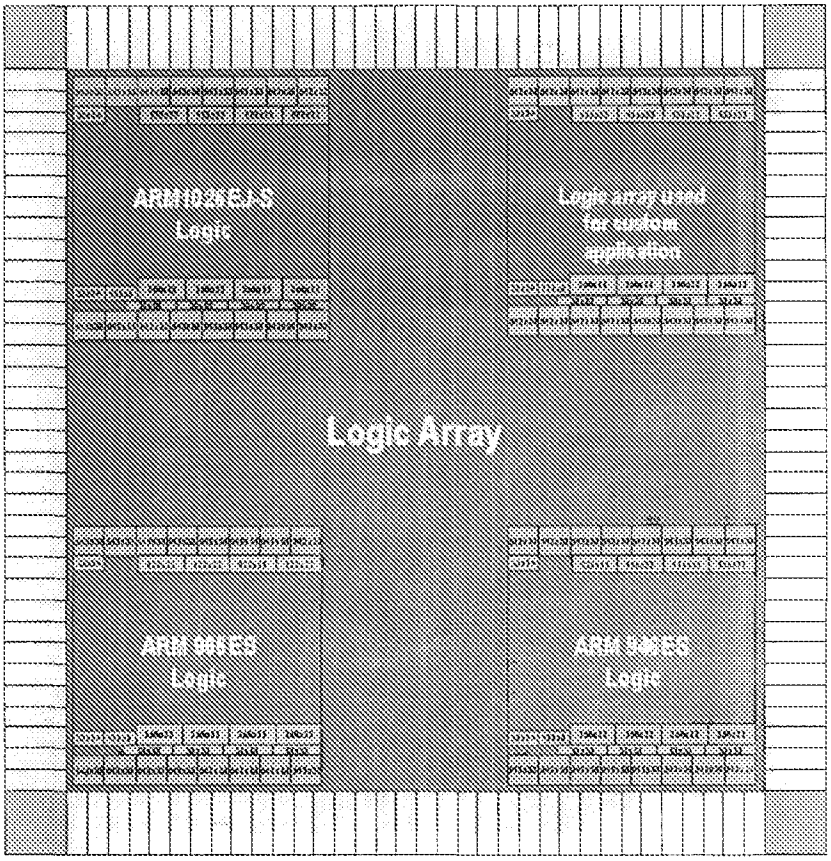


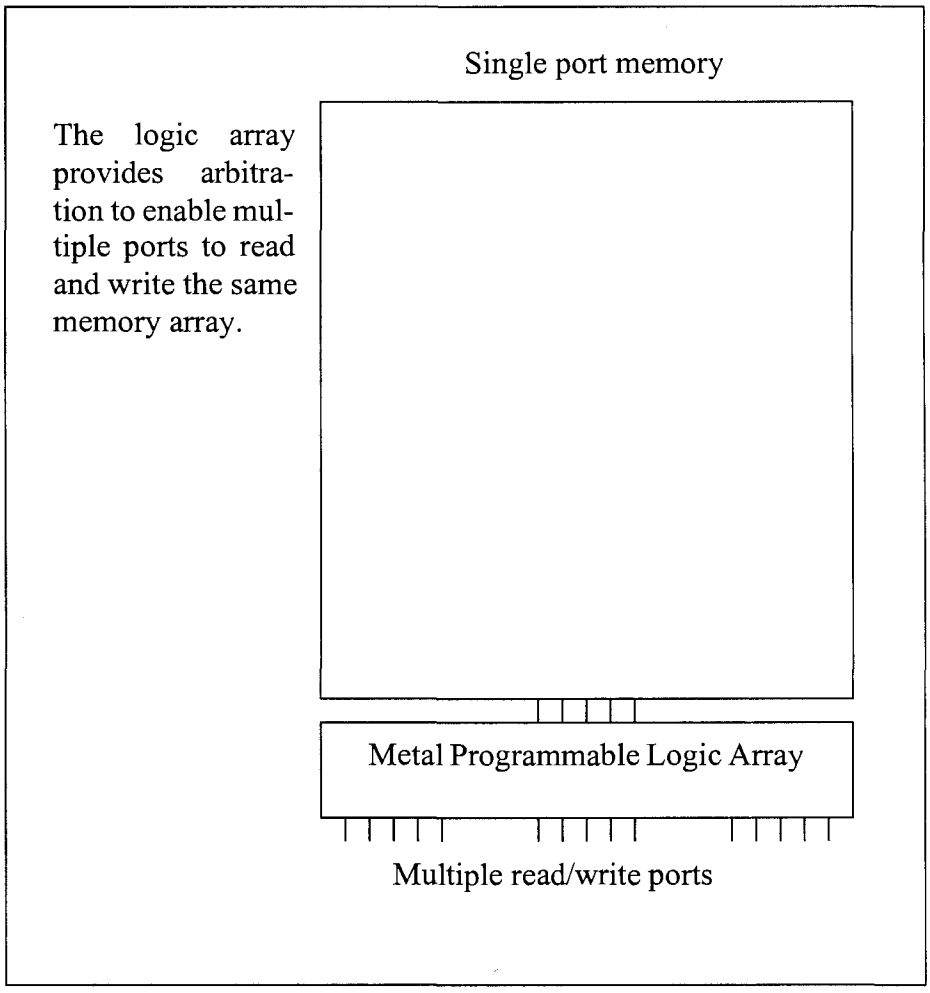
Figure5.8 Example of how this function could be used in a chip



5.2.2 Multi-port memory

A multi port memory can be mapped onto a single port memory block. This is accomplished by programming the logic array to create multiple memory read/write ports and arbitrating between them. In the following examples, a large single port memory is embedded in the base array. How this memory is used is determined by how the logic array is programmed.

Figure5.8 Multi-Port Memory Example

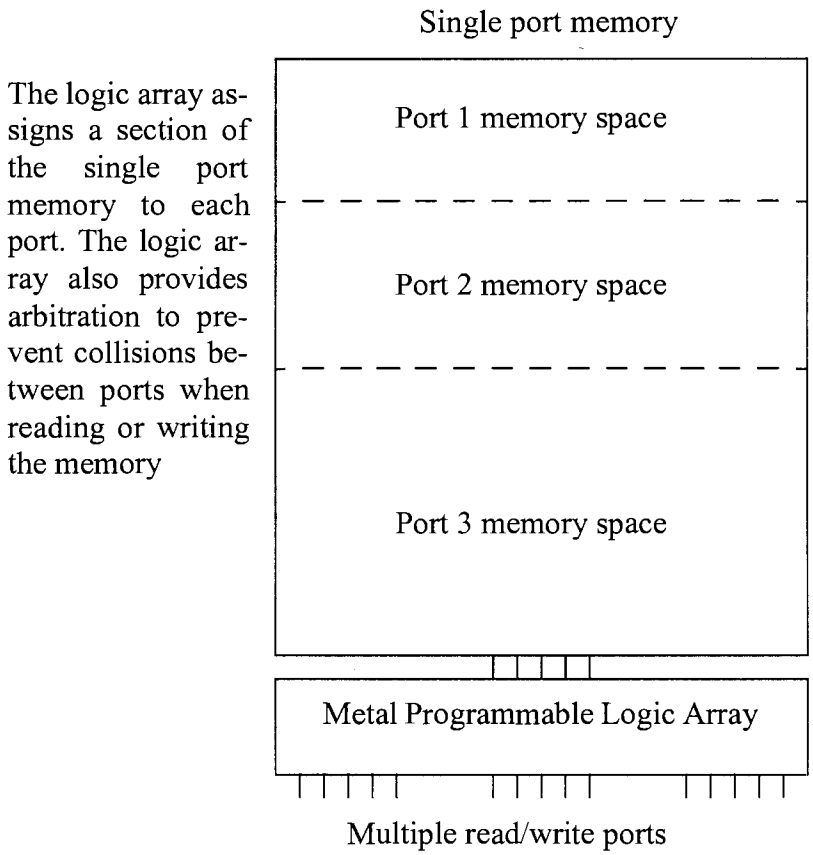


5.2.3 Multiple single port memories

Multiple single port memories can be mapped to one single port memory. This is accomplished by programming the logic array to break up the address space of a given single port memory into multiple blocks that are

accessible from different read/write ports. The logic array will perform arbitration between the ports.

Figure5.9 Multiple Single Port Memory Example



5.3 Advantages of Invention

Efficient use of available memory and logic resources is achieved. The memory resources are fixed, but this invention outlines how they can be used in different ways to take full advantage of them.

5.4 Alternate ways to make and use invention

5.5 Disadvantages of Invention